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14. ABSTRACT

The original scope this project was reduced to reflect personnel changes and a significant budget reduction. In its modified version the project aimed at initial development of test structures, testing methods, and physics-based device models for reliability assessment of novel GaN power switches. Only commercially available GaN devices (from EPC) were available to the team and some of the testing and method development also utilized commercially available Si and SiC power switch devices. Testing set-ups and methods were established /developed for temperature-dependent I-V measurements, high-temperature reverse-bias measurements, and dv/dt testing. Possibilities for single event burnout testing were examined as well. Device simulation under the conditions of some of the testing was performed on Silvaco TCAD software using device models that were developed following published work on GaN HEMT switches. The examined devices were found to match or exceed the specifications. Undesirable switching (latching) of enhancement-mode devices under blue light were observed.

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Final Report

Reliability Assessment of GaN Power Switches

Reporting Period: **March 1, 2013 – December 31, 2014**

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Submitted by

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According to the statement of work for the continuation of the University of Toledo research grant "Reliability Assessment of GaN Power Switches", this project aimed at initial development of test structures, testing methods, and physics-based device models for reliability assessment of novel GaN power switches, which had been developed earlier under the DARPA programs. The plan of work included the following items:

1. Preliminary review of prime contractors' process technologies needed for the development of test structures.
2. Preliminary test structure development.
3. Purchase/installation/training related to the software packages needed for the project (e.g., Silvaco TCAD Mixed Mode 2D Simulator and SABER Circuit Simulator).
4. Generate preliminary simulation data.
5. Acquire and install the test equipment.
6. Acquire commercial GaN and SiC devices for test validation.
7. Preliminary test data collection for test circuit validation: static I-V and C-V, high-temperature reverse-bias (HTRB) and single electron burnout (SEB) tests.
8. Refine test structures, circuits, and procedures, and, if possible, develop standardized test structures.

The project team consisted of three faculty members from the Department of Electrical Engineering and Computer Science and two graduate research assistants at the M.S. level, whose thesis research was directly related to this project. In addition, undergraduate students were involved over shorter periods of time to assist in software installation, testing, and coding (LabView and Matlab).

The original scope this project (originally awarded to and Krishna Shenai as the PI, who also started work on the project in early 2013) was reduced to reflect personnel changes and a significant budget reduction (only part of the original 1st year budget was preserved as funding for this modified version of the project). At the beginning of this modified version of the project, it became clear that the team would not have access to any devices developed and fabricated under DARPA or other institutions, so only commercially available GaN devices (mainly from Efficient Power Conversion corporation, EPC) were available to the team. Some of the testing/verification work and method development also utilized commercially available Si and SiC power switch devices.

Testing and Measurements Results

The specific gallium nitride transistors tested are enhancement (normally-off) HEMT (advanced field effect transistor) devices from Efficient Power Conversion (EPC) Corporation. These devices are in passivated die form, with land grid array solder bars. The electrical measurements were performed either on individual devices placed on the thermal chuck of a probe station (by Micromanipulator, acquired as part of this project) or on devices mounted on printed circuit boards as part of testing circuits that were designed and fabricated in this project. The testing/measurement configurations included various units such as sources, oscilloscopes, and probes which were either

acquired as part of this project, or were already available in our research lab. The measurements were performed using computer-controlled use of the sources and units as well as data acquisition based on LabView and/or Matlab.

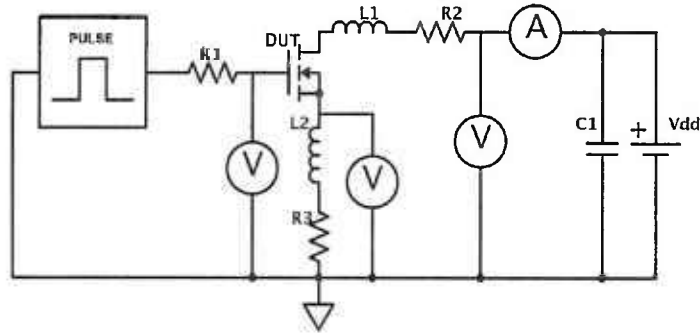


Fig. 1. EPC2012 passivated die Fig. 2. Diagram of I-V characterization via pulsed method

For the *I-V measurements*, the gallium nitride device was mounted on a printed circuit board. The I-V characteristic was compared to that of conventional devices, such as silicon and silicon carbide, at low and high temperatures. The I-V characteristic of gallium nitride shows an on-resistance lower than silicon or silicon carbide devices.

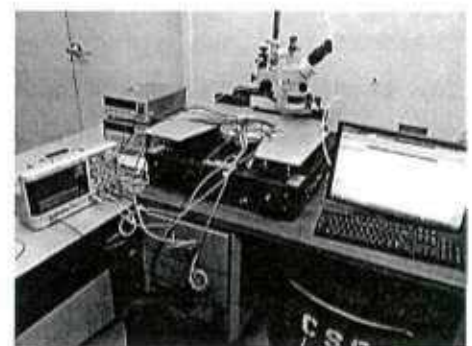
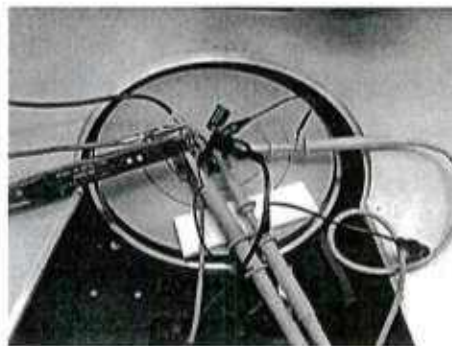


Fig. 3. (left) EPC2012 mounted on a PCB. There is a copper connection to each of the device terminals; (middle) the PCB with the DUT facing down on the chuck and under some pressure; (right) the entire system in operation.

Gallium nitride devices are also found to saturate at far lower drain-source voltages than the example silicon and silicon carbide devices, and require a lower gate voltage to turn on fully, which means that lower supply voltages are necessary to take full advantage of the device. The gallium nitride characteristic did have a greater sensitivity to temperature than the conventional devices, however.

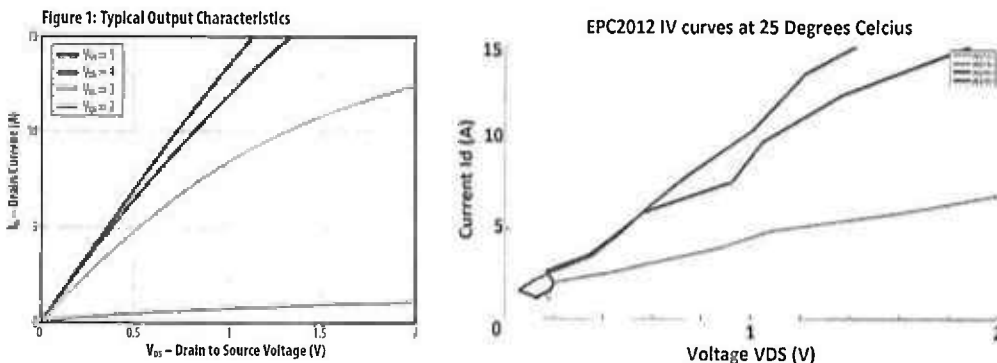


Fig. 4. (left) Manufacturer I-V curve (from datasheet); (right) our I-V curve.

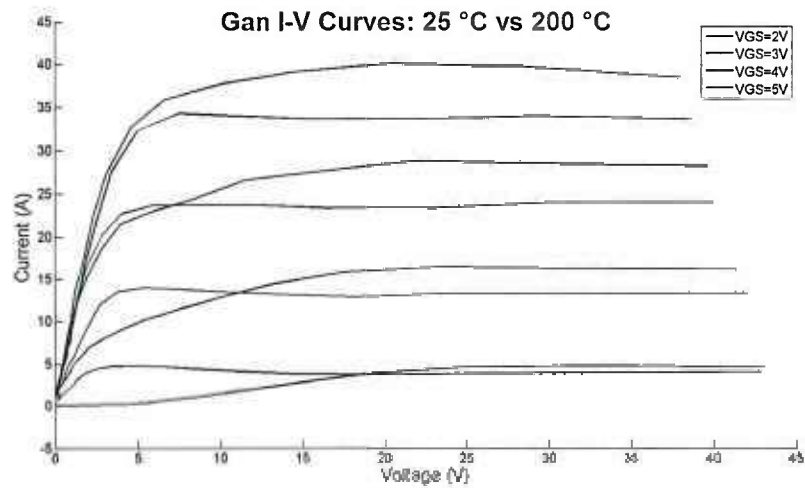


Fig.5. Measured I-V curves for mounted EPC2012 at two temperatures.

The drain-source leakage current of gallium nitride devices was also compared to conventional devices, from low to high temperatures. The leakage current for gallium nitride devices was many orders of magnitude higher than the conventional (Si and SiC) devices tested as illustrated by the figures below.

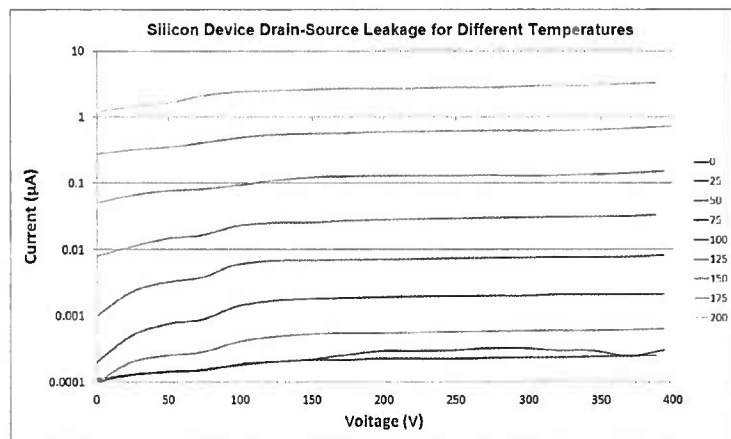
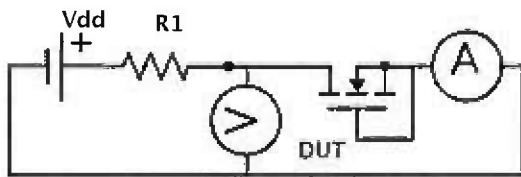
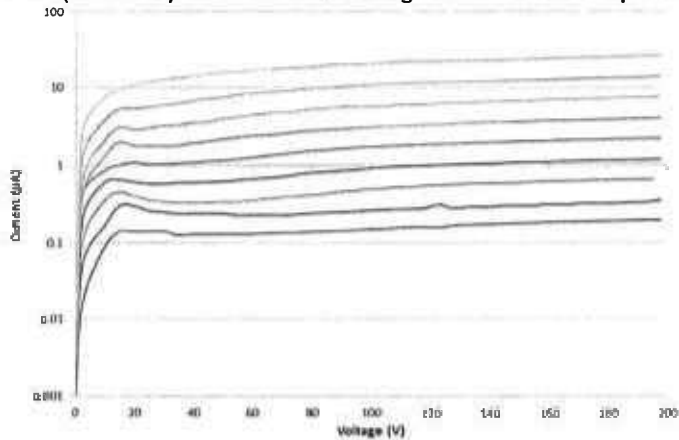


Fig. 6. The circuit diagram of the high-temperature reverse-bias (HTRB) leakage test and results for a Si device (IRF710).

GaN (EPC2012) Drain-Source Leakage for Different Temperatures



GaN (EPC2001) Drain-Source Leakage for Different Temperatures

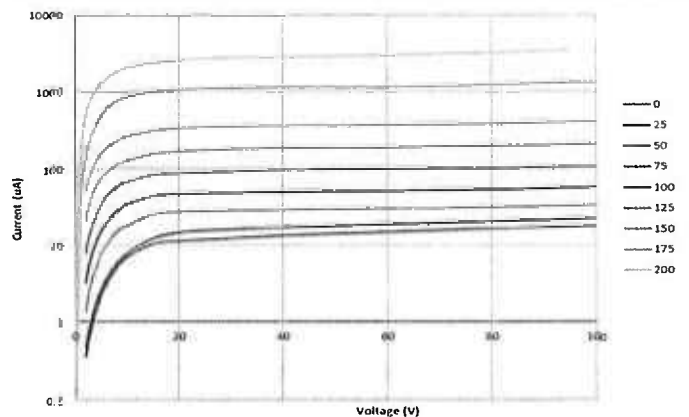


Fig. 7. GaN leakage current for different temperatures for two devices (left) EPC2012, (right) EPC2001

Gallium nitride has superior dv/dt immunity when compared to conventional devices. The device tested withstood a dv/dt magnitude that was double the maximum dv/dt the conventional devices could withstand. The theoretical dv/dt immunity level of gallium nitride devices is nearly ten times the level of conventional devices and our set-up was not able to test at dv/dt values of more than 15 V/ns (12V/ns in Fig.9 below).

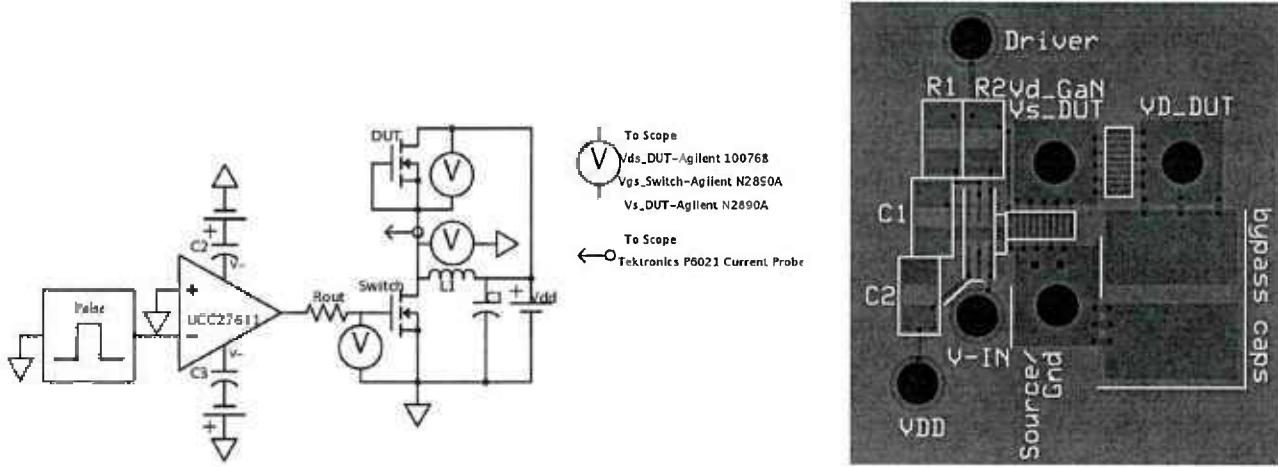


Fig. 8. Schematic of dv/dt Test and the board design

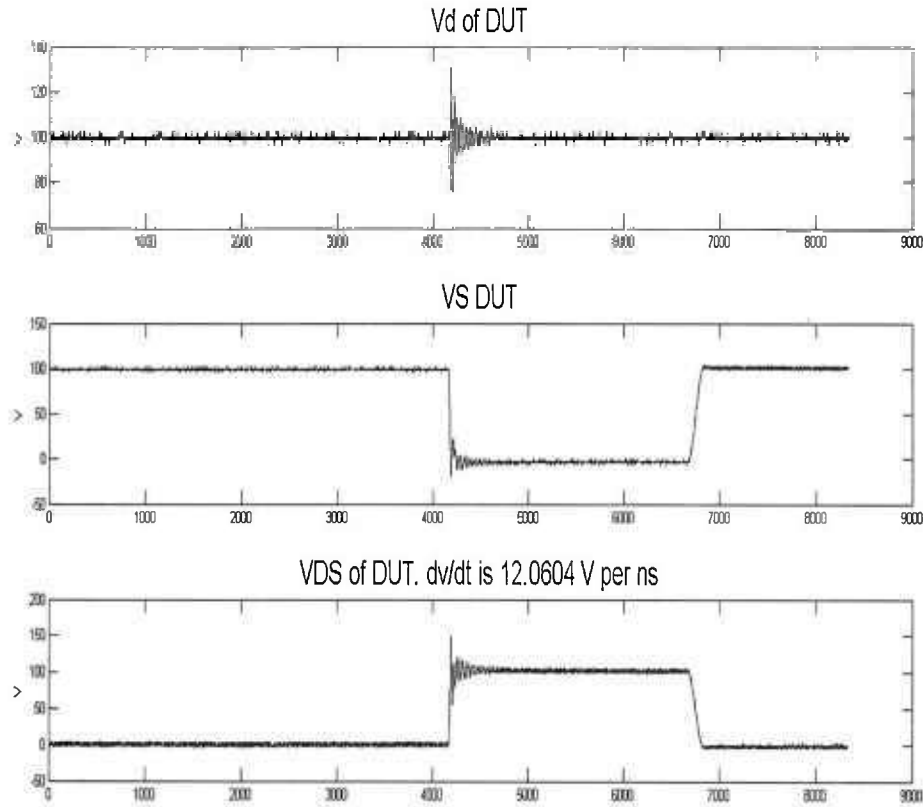


Fig.9. dv/dt as extracted from Matlab acquired data: (top) drain voltage of DUT; (middle) source voltage of DUT; (bottom) difference between drain and source voltages of DUT, with dv/dt calculated and displayed.

Gallium nitride devices have very good resistance to radiation. Tests done by the manufacturer show that gallium nitride devices can withstand larger amount of radiation than conventional power devices, and have no unwanted effects. In the testing performed in this project, a bank of gallium nitride devices had a high drain-source voltage and were turned off. After hundreds of hours, no single event occurred and the devices did not turn on or break at any point.

As part of this testing, a substantial increase in the parasitic current was observed upon exposure of the unpackaged device to continuous wave blue laser light. Even more interestingly, after removal of the laser light, the elevated current levels remained, revealing latching effect that has not been observed before in these devices. This undesirable latching effect needs further studies to understand and prevent, or even use in potential applications. A summary of the observed results is given in the table below.

Device	VDS Max (V)	IDSS before laser (μ A)	IDSS after laser (mA)
EPC2001	100	0.5-15	0.5-10
EPC2012	200	0.1-1	0.5-5
EPC2014	40	30-50	0.5-5

Silvaco Device Modeling

Silvaco TCAD OMNI license software was purchased as part of this project and was used to design and simulate GaN HEMT devices. Since the device structure and material details of the EPC devices was not available, we examined the literature to identify published work that provides enough details on devices that appear as close as possible to the EPC devices used in our measurements (as discussed above). An example of output I-V characteristics generated from a device designed according to the information provided in a reference (I. Hwang, H. Choi and J. W. Lee, "1.6 kV, 2.9 m cm² normally off p-GaN HEMT device," in in Proc. 24th Int. Symp. Power Semiconductor Devices, Bruges, Jun. 2012.) is shown below in Fig.10.

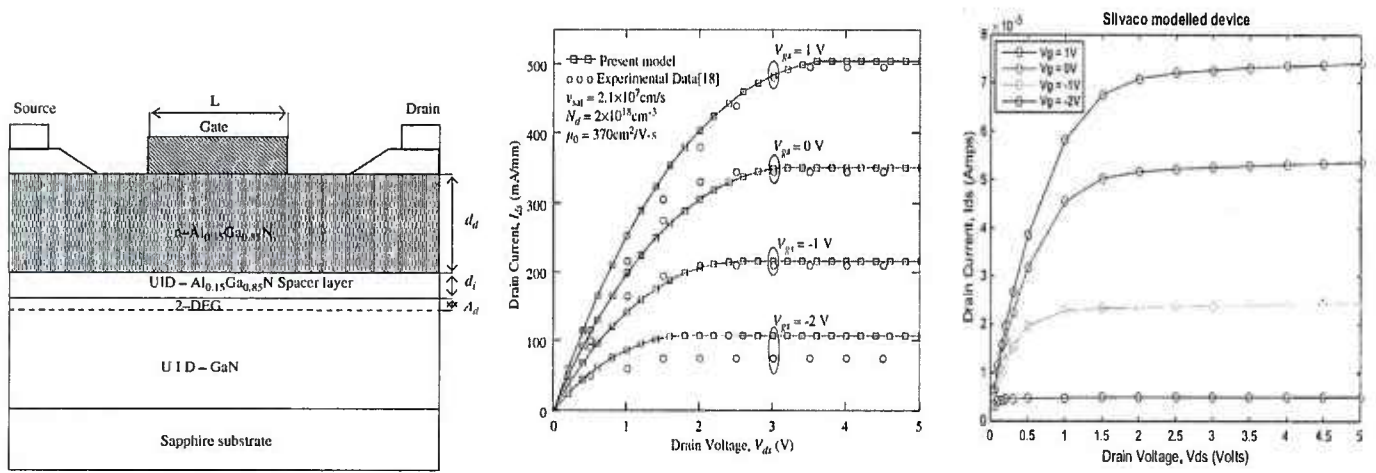


Fig.10. The device structure and its I-V characteristics as provided by a journal paper (middle) and according to Silvaco modelled device (right).

Various types of GaN HEMT devices were designed and modeled, including depletion mode devices and enhancement mode devices with emphasis on the latter. Besides basic Schottky gate enhancement mode devices, recessed-gate devices and field-plate structures were examined. Some details on a recessed-gate device, which was found to match the EPC devices (such as the EPC2012, although EPC devices are likely not of this type) to some degree, are provided in the example (table and the figures) below.

Material Properties	Device values
AlGaIn doping (n doped)	$3.7 \times 10^{17} \text{ cm}^{-3}$ (Moderately doped)
GaN doping (n doped)	$3.7 \times 10^{13} \text{ cm}^{-3}$ (Lightly doped)
Aluminum composition in AlGaIn	20%
GaN mobility	$1370 \text{ cm}^2/\text{v.s}$
Thickness of AlGaIn layer	10 nm
Thickness of GaN layer	600 nm
Gate contact	Schottky
Work function of Schottky gate	6.3 eV

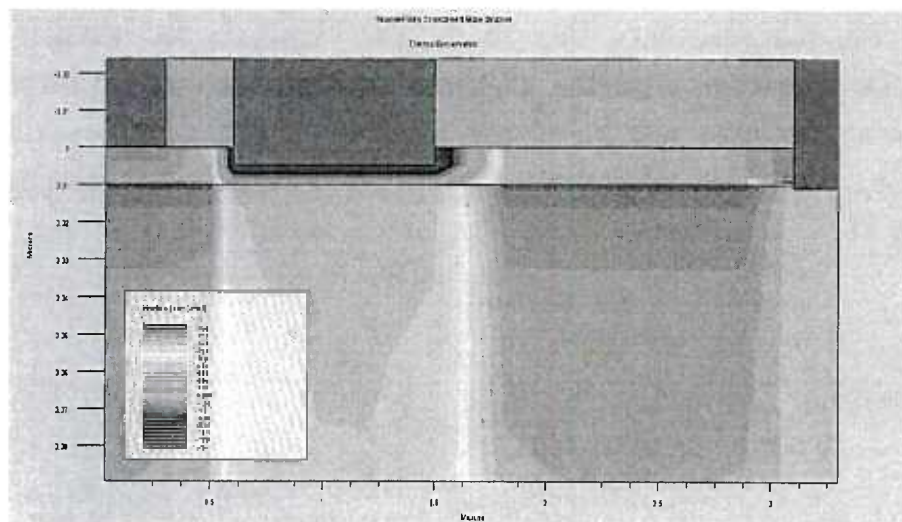


Fig. 11. Electron concentration in an enhancement mode recessed gate HEMT (zoomed at the interface)

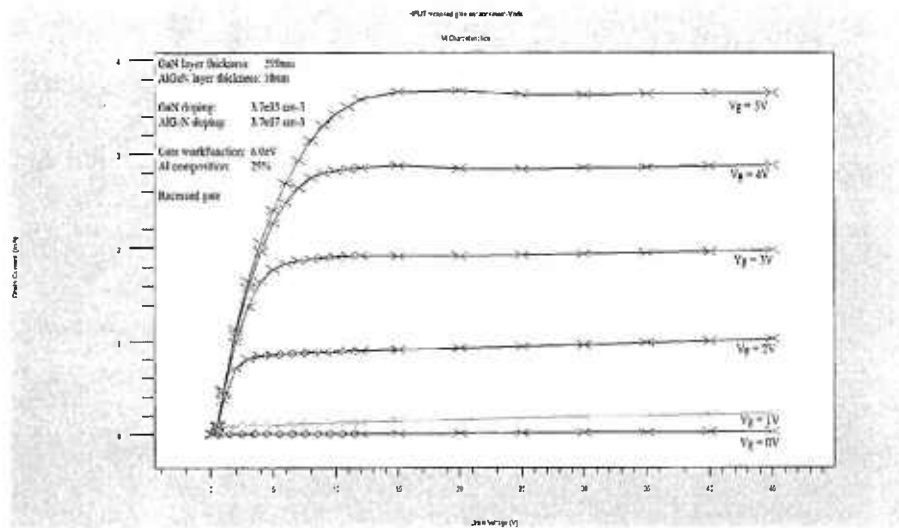


Fig. 12: Recessed gate HEMT enhancement mode I-V characteristics.

Temperature dependences were also examined and both temperature dependent I-V curves and the HTRB simulation data were obtained and compared to the measured data on EPC devices. While some general similarities and parallels were observed, due to the (most likely) different device design and material details, we could not draw any substantial conclusions based on that.

The devices designed (and simulated) in Silvaco's Atlas software can be exported to the circuit simulator Silvaco 2D Mixed Mode and the performance of specific test circuits can be verified. This was done for some of the designed devices and some of the very basic circuits used in the measurements, but again a comparison with the testing results with EPC was not found to be meaningful due to the fact that the simulated devices (and their circuit models extracted by Silvaco) do not represent the actual EPC devices used in the measurements. However, we are confident that the sequences we have used in such modeling can be successfully applied to simulate devices with known designs such as state-of-the-art ones that are being developed at various institutions.

As a result of this project a basic facility equipped with a probe station with a thermal chuck and various source and measurement units (all which are computer-controlled) was established and can be used in other projects. A level of expertise in the area of device testing and modeling was developed and two graduate students were able to complete their M.S. thesis research. One of them, Shams Faruque, defended his thesis in Fall 2014 and was recently offered a job at Boeing (at their St. Louis location) and another, Sreeram Jogi, is expected to graduate in May 2015.